**WHAT IS CLAIMED IS:**

1. An input/output node for a computer system, said input/output node comprising:

a transceiver unit implemented on an integrated circuit chip, wherein said transceiver unit is configured to receive and transmit packets on a point-to-point link of a packet interface;

a graphics engine implemented on said integrated circuit chip, wherein said graphics engine is coupled to receive graphics packets received by said transceiver unit and is configured to render digital image information in response to receiving said graphics packets; and

an I/O hub implemented on said integrated circuit chip, wherein said I/O hub is coupled to receive I/O packets corresponding to packets received by said transceiver unit and is configured to initiate bus cycles corresponding to said I/O packets upon a peripheral bus.

2. The input/output node as recited in claim 1 further comprising an interface unit implemented on said integrated circuit chip, wherein said interface unit is coupled to said transceiver unit and is configured to convey packets between said transceiver unit and each of said graphics engine and said I/O hub.

3. The input/output node as recited in claim 1 further comprising a graphics bus interface implemented on said integrated circuit chip, wherein said graphics bus interface is coupled to receive and to translate said graphics packets into graphics commands suitable for transmission upon a graphics bus.

4. The input/output node as recited in claim 1, wherein said I/O hub is further configured to receive peripheral transaction bus cycles from said peripheral bus and to transmit packets corresponding to said peripheral transaction bus cycles to said transceiver unit.

5. The input/output node as recited in claim 1, wherein said graphics engine includes a configuration register, wherein said configuration register provides a user selectable bit for enabling and disabling said graphics engine.

6. The input/output node as recited in claim 1, wherein said graphics engine is further configured to translate said digital image information into packets suitable for transmission upon said point-to-point link of a packet interface.

7. The input/output node as recited in claim 1, wherein said point-to-point link of a packet interface is a point-to-point HyperTransport™ link including a first set of uni-directional wires and a second set of uni-directional wires each configured to convey packets including control packets and data packets, wherein said control packets include command packets, info packets and response packets and wherein said control packets and data packets share the same wires.

8. The input/output node as recited in claim 7, wherein said I/O hub is coupled to receive said I/O packets via a HyperTransport™ link.

9. The input/output node as recited in claim 1, wherein said I/O hub is coupled to receive said I/O packets via an internal packet bus.

10. A computer system comprising:

a processing node including one or more processors;

a link of a packet interface coupled to said processing node;

an input/output node coupled to said link, said input/output node including:

a transceiver unit implemented on an integrated circuit chip, wherein said transceiver unit is configured to receive and transmit packets on a point-to-point link of a packet interface;

a graphics engine implemented on said integrated circuit chip, wherein said graphics engine is coupled to receive graphics packets received by said transceiver unit and is configured to render digital image information in response to receiving said graphics packets; and

an I/O hub implemented on said integrated circuit chip, wherein said I/O hub is coupled to receive I/O packets corresponding to packets received by said transceiver unit and is configured to initiate bus cycles corresponding to said I/O packets upon a peripheral bus.

11. The computer system as recited in claim 10, wherein said input/output node further comprising an interface unit implemented on said integrated circuit chip, wherein said interface unit is coupled to said transceiver unit and is configured to convey packets between said transceiver unit and each of said graphics engine and said I/O hub.

12. The computer system as recited in claim 10, wherein said input/output node further comprising a graphics bus interface implemented on said integrated circuit chip, wherein said graphics bus interface is coupled to receive and to translate said graphics packets into graphics commands suitable for transmission upon a graphics bus.

13. The computer system as recited in claim 10, wherein said I/O hub is further configured to receive peripheral transaction bus cycles from said peripheral bus and to transmit packets corresponding to said peripheral transaction bus cycles to said transceiver unit.

14. The computer system as recited in claim 10, wherein said graphics engine includes a configuration register, wherein said configuration register provides a user selectable bit for enabling and disabling said graphics engine.

15. The computer system as recited in claim 10, wherein said graphics engine is further configured to translate said digital image information into packets suitable for transmission upon said point-to-point link of a packet interface.

16. The computer system as recited in claim 10, wherein said point-to-point link of a packet interface is a point-to-point HyperTransport™ link including a first set of uni-directional wires and a second set of uni-directional wires each configured to convey packets including control packets and data packets, wherein said control packets include command packets, info packets and response packets and wherein said control packets and data packets share the same wires.

17. The computer system as recited in claim 16, wherein said I/O hub is coupled to receive said I/O packets via a HyperTransport™ link.

18. The computer system as recited in claim 10, wherein said I/O hub is coupled to receive said I/O packets via an internal packet bus.

19. An input/output node for a computer system, said input/output node comprising:

a transceiver unit implemented on an integrated circuit chip, wherein said transceiver unit is configured to receive and transmit packets on a point-to-point link of a packet interface;

a graphics bus interface implemented on said integrated circuit chip, wherein said graphics bus interface is coupled to receive packets including graphics commands and to translate said packets into graphics commands suitable for transmission upon a graphics bus.

a graphics engine implemented on said integrated circuit chip and coupled to said graphics bus, wherein said graphics engine is coupled to receive said graphics commands via said graphics bus and is configured to render digital image information in response to receiving said graphics commands; and

an I/O hub implemented on said integrated circuit chip, wherein said I/O hub is coupled to receive I/O packets corresponding to packets received by said transceiver unit and is configured to initiate bus cycles corresponding to said I/O packets upon a peripheral bus.

20. The input/output node as recited in claim 19 further comprising an interface unit implemented on said integrated circuit chip, wherein said interface unit is coupled to said

transceiver unit and is configured to convey packets between said transceiver unit and each of said graphics engine and said I/O hub.

21. The input/output node as recited in claim 19, wherein said I/O hub is further configured to receive peripheral transaction bus cycles from said peripheral bus and to transmit packets corresponding to said peripheral transaction bus cycles to said transceiver unit.

22. The input/output node as recited in claim 19, wherein said graphics engine includes a configuration register, wherein said configuration register provides a user selectable bit for enabling and disabling said graphics engine.

23. The input/output node as recited in claim 19, wherein said graphics engine is further configured to translate said digital image information into packets suitable for transmission upon said point-to-point link of a packet interface.

24. The input/output node as recited in claim 19, wherein said point-to-point link of a packet interface is a point-to-point HyperTransport™ link including a first set of uni-directional wires and a second set of uni-directional wires each configured to convey packets including control packets and data packets, wherein said control packets include command packets, info packets and response packets and wherein said control packets and data packets share the same wires.

25. The input/output node as recited in claim 24, wherein said I/O hub is coupled to receive said I/O packets via a HyperTransport™ link.

26. The input/output node as recited in claim 19, wherein said I/O hub is coupled to receive said I/O packets via an internal packet bus.